ABSTRACT OF THE DISCLOSURE

In a semiconductor memory device, there are provided refresh timers issuing refresh requests at different periods, and refresh address generation circuits generating refresh addresses in accordance with the respective refresh requests. In a row select circuit, it is set for each row according to which, of the refresh addresses different from each other in issuance period, a corresponding word line is to be selected. Each word line can be refreshed in a different refresh cycle, and only a word line of pause refresh failure is refreshed in a shorter cycle while the other word lines are refreshed in a longer cycle. Current dissipation can be reduced in a self-refresh mode.